APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/944,993	08/30/2001	Anthony Moschopoulos	703.155US1	1856

21186	7590	06/23/2005		

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. BOX 2938
MINNEAPOLIS, MN 55402-0938

EXAMINER
CHOI, WOO H

ART UNIT	PAPER NUMBER
2189	

DATE MAILED: 06/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)
	09/944,993	MOSCHOPOULOS, ANTHONY
Office Action Summary	Examiner	Art Unit
	Woo H. Choi	2189

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed
  after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any
  earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _13 April 2005_.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is
closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _1-46_ is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) _1-46_ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage
application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☐ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
    Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____ .

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

DETAILED ACTION

Claim Objections

1.   Claim13 is objected to because of the following informalities: The limitation "inversion

bit is set **than**" in line 8 should be changed to "inversion bit is set then." Appropriate correction

is required.

Claim Rejections - 35 USC § 112

2.   The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making
> and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it
> pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode
> contemplated by the inventor of carrying out his invention.

3.   Claims 1 – 46 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with

the written description requirement. The claim(s) contains subject matter which was not

described in the specification in such a way as to reasonably convey to one skilled in the relevant

art that the inventor(s), at the time the application was filed, had possession of the claimed

invention. All of the independent claims were amended to require the data source to either

perform various acts or include structures to perform acts claimed in the method claims. The

specification does not support these amended limitations. The figures containing the flow charts

clearly show that the claimed acts are performed outside the data source. Figures illustrating the

claimed structures clearly show that the data source is separate from the controller, the temporary

circuit and other circuits associated with bit inversions. The Examiner asks Applicant to

specifically point out where in the specification the newly added limitations are supported.

Claim Rejections - 35 USC § 102

4.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the

basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on
sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed
in the United States before the invention by the applicant for patent or (2) a patent granted on an application for
patent by another filed in the United States before the invention by the applicant for patent, except that an
international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this
subsection of an application filed in the United States only if the international application designated the United
States and was published under Article 21(2) of such treaty in the English language.

5.   Claims 1 – 5, 7 – 9, 13 – 18, 21, 23 and 25 – 27 are rejected under 35 U.S.C. 102(e) as

being anticipated by de la Iglesia *et al.* (US Patent No. 6,490,703, hereinafter "de la Iglesia").

6.   With respect to claims 1, 13 and 17, de la Iglesia discloses a method of transferring a data

stream (figure 8) comprising:

transferring a plurality of bits associated with a data stream from a data source (figure 5,

processor 304 and memory interface 400, see also figure 8, step 808) to a temporary storage

(figure 5, memory 306, figure 8, step 818);

concurrently intercepting during the transfer and on or within the data source, each bit

associated with the data stream and counting a bit-transfer total and a bit-set total associated with

the data stream (figure 8, step 810); and

determining, on or within the data source, if the bit-set total exceeds more than half the

bit-transfer total (steps 810, col. 9 lines 26 – 31) and if so setting an inversion flag bit which is

associated with the data stream (step 816, see also figure 2 and col. 14 – 27, flip bits indicate the

state of data inversion).

7.   With respect to claim 2 and 18 the method further comprises:

transferring from the temporary storage to a target source each bit associated with the

data stream and concurrently inverting each bit as transferred, if the inversion flag bit is set

(steps 818 – 828, if the bits stored in the memory 306 are inverted in step 814, they are recovered

in step 826 by inverting again).

8.   With respect to claim 3, the method further comprises:

shifting the inversion flag bit to a flag storage (818, flag bits are stored or "shifted" to

memory).

9.   With respect to claims 4 and 14, the method further comprises:

assembling one or more additional inversion flag bits in the flag storage, each additional

inversion flag bit associated with a single additional data stream; and

maintaining each additional data stream in the temporary storage (figure 8, the process of

data word inversion determination and the storage of an inverted data word with flip bits occurs

for every 64 bit data word with memory storing a plurality of data words with the associated flip

bits).

10.   With respect to claim 5, 15 and 16, the method further comprises:

transferring from the temporary storage to a target source each bit associated with the

data stream and each of the additional data streams while concurrently inverting each transferred

bit, if the inversion flag bit associated with a transferred data stream is set, as identified in the

flag storage (steps 818 – 828, see rejection of claim 2 above).

11.   With respect to claims 7 and 21, de la Iglesia discloses a method of transferring a data

stream (figure 8), comprising:

        receiving a data stream and an inversion flag associated with the data stream from a data

source;

        transferring one or more bits associated with the data stream from a data source to a

target source, if the inversion flag is unset; and

        inverting, on or within the data source (figure 5, 304, 400), the bits associated with the

data stream as the data stream is transferred from the data source to the target source, if the

inversion flag is set (steps 820 – 828).

12.   With respect to claim 8 the inversion flag and the data stream are stored together in the

data source (step 818, flop bits and data are both stored in the memory).

13.   With respect to claim 9 the inversion flag and the data stream are separately stored in the

data source (flip bits and data occupy separate spaces in the memory).

14.   With respect to claim 23, the controller acquires the inversion bit by stripping the

inversion bit from the data stream (figure 8, steps 818 – 824).

15.   With respect to claim 25, de la Iglesia discloses system for transferring a data stream,

comprising:

    a control buffer (figure 5, 304, processor registers and other processor storage resources);

    a storage buffer (306);

    an inversion storage (306, memory stores data as well as inversion bits);

    a counting set of executable instructions to count set bits associated with a data stream

being received from the control buffer into the storage buffer as the storage buffer receives the

data stream from a data source (figure 5, computer 300), and the counting set of executable

instructions generates an inversion bit associated with the data stream, wherein the inversion bit

is housed in the inversion storage and is set if a total number of set bits exceeds more than half a

total number of bits associated with the data stream (figure 8, 810), and wherein the counting set

of instructions, the control buffer, the inversion storage, and the storage buffer are included

within the data source (figure 5, 300).

16.   With respect to claim 26, the system further comprises:

    a transfer set of executable instructions operable to use the counting set of executable

instructions to transfer the data stream from the storage buffer to a target device, wherein the

entire data stream is inverted if the inversion bit is set as the data stream is being transferred to

the target device (824 – 828).

17.   With respect to claim 27, the inversion bit is transferred with the data stream to the target

device (816).

18.   Claims 1 – 7, 9 – 12, 19 – 22, 24 – 26, 28 – 37, 39 – 41 and 44 – 46 are rejected under 35

U.S.C. 102(b) as being anticipated by Norman (US Patent No. 5,873,112).

        With respect to claims 7, 11, 12, 21, 28, 32, 33 and 36, Norman discloses a method of

transferring a data stream (col. 18, lines 29 – 65), comprising:

        receiving a data stream (col. 18, lines 46 – 56) and an inversion flag (col. 18, lines 30 –

33) associated with the data stream from a data source (figure 3, memory chip 3, figure 7, 429

and 416);

        transferring one or more bits associated with the data stream from a data source to a

target source (figure 7, 401), if the inversion flag is unset; and

        inverting, on or with the data source, the bits associated with the data stream as the data

stream is transferred from the data source to the target source, if the inversion flag is set (col. 18,

lines 46 – 56).

19.   With respect to claim 8, the inversion flag and the data stream are stored together in the

data source (polarity bits or inversion flags are stored in the flash array).

20.   With respect to claims 9 and 24, inversion flag and the data stream are separately stored

in the data source (col. 18, lines 30 – 33, polarity bits for an entire sector are stored separately

from the actual data sector).

21.   With respect to claim 10, the inversion flag is stored with one or more additional

inversion flags as a single data structure in the data source, each additional inversion flag

associated with an additional data stream (see rejection of claim 9 above, polarity bits are for an

entire sector are stored together with one bit representing one data packet).

22.   With respect to claim 22, the system further comprises:

        a temporary storage (figure 3, 104) operable to house the data stream as the data stream is

acquired from the data source device; and

        a register storage (figure 3, 118) operable to house the inversion bit as the data stream is

acquired from the data source device.

23.   With respect to claim 29 – 31, and 34, the apparatus further comprises:

        a buffer (figure 3, 104) to house the packet prior to transfer; and

        a register (118) to house the inversion bit.

24.   With respect to claim 35, the state machine is configured by interfacing one or more

electro-mechanical devices (216 and other circuits, see page 3 of the specification, Applicant

seems to regard any semiconductor type of devices to be electro-mechanical devices).

25.   With respect to claim 37, the data packet is a fixed length data packet (figure 2).

26.   With respect to claim 39, the apparatus is a flash memory device (figure 3, 216).

27.   With respect to claims 1, 19, Norman discloses an inversion data transfer system (figure

7), comprising:

        a data source device including a temporary storage and a controller (401 and 429 and

416);

        a temporary storage (416); and

        a controller (429) that transfers a data stream having a plurality of bits from the data

source device to the temporary storage, and concurrent to the transfer determines if a total

number of set bits within the data stream is more than half of a total number of bits associated

with the data stream, and if so associating a set inversion bit with the data stream, otherwise

associating an unset inversion bit with the data stream (see also abstract and claim 1, and

discussions related to figure 3); and

        a register storage operable to house the inversion bit and one or more additional inversion

bits, wherein each additional inversion bit is associated with an additional data stream (figure 3,

118, col. 15, lines 65 – 67 and col. 17, lines 50 – 54).

28.   With respect to claims 2 – 6 and 20, the controller further retrieves from the register

storage each inversion bit associated with a transferred data stream and is operable to

concurrently transfer the transferred data stream from the temporary storage and invert the bits

associated with the transferred data stream if the inversion bit is set (col. 18, lines 29 – 56).

29.   With respect to claim 25, Norman discloses a system for transferring a data stream,

comprising:

        a control buffer (figure 7, 401, host memory which is inherent in the host processor of

figure 7);

        a storage buffer (figure 7, 416);

        an inversion storage (figure 3, 118);

        a counting set of executable instructions to count set bits associated with a data stream

being received from the control buffer into the storage buffer as the storage buffer receives the

data stream from a data source (figure 7, 401,429 and 416), and the counting set of executable

instructions generates an inversion bit associated with the data stream, wherein the inversion bit

is housed in the inversion storage and is set if a total number of set bits exceeds more than half a

total number of bits associated with the data stream (abstract), and wherein the counting set of

instructions, the control buffer, the inversion storage, and the storage buffer are included within

the data source (see figure 7).

30.   With respect to claim 26, the system further comprises:

        a transfer set of executable instructions operable to use the counting set of executable

instructions to transfer the data stream from the storage buffer to a target device, wherein the

entire data stream is inverted if the inversion bit is set as the data stream is being transferred to

the target device (col. 18, lines 29 – 56).

31.   With respect to claims 40 and 41, Norman discloses a flash memory device (figure 3),

comprising:

    a temporary storage (104);

    a receiving controller(102);

    a counting controller (claim 24, col. 26, lines 26 – 34); and

    a transferring controller that transfers a data packet received by the receiving controller in

a temporary storage to a target device and further inverts the data packet during the transfer if the

counting controller indicates to the transferring controller that the packet requires inversion

(claims 24 and 25, col. 26, lines 40 – 53).

32.   With respect to claim 44, the counting controller includes a packet based ones counter

(col. 13, line 45 – col. 19, line 64).

33.   With respect to claim 45, the device further comprises a shift-load register (figure 3, 118)

used to house an inversion bit generated by the counting controller, wherein the inversion bit, if

set, indicates the data packet is to be inverted.

34.   With respect to claim 46, one or more multiplexors (Figure 3, 106), the shift-load register

(118), and the temporary storage (104) are used by the transferring controller to transfer the data

packet.

Claim Rejections - 35 USC § 103

35.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in
> section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are
> such that the subject matter as a whole would have been obvious at the time the invention was made to a person
> having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the
> manner in which the invention was made.

36.   Claims 38, 42 and 43 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Norman in view of Goldtein (US Patent Application Publication No. 2003/0028672).

Norman discloses all of the limitations of the parent claims as discussed above.

However, Norman does not specifically disclose specific applications of his inventions in a

digital camera system that uses a compact flash memory. Variable size packet is not disclose by

Norman either. On the other hand, Goldstein discloses a digital camera system (figure 2A) and

Compact Flash card (page 1, paragraph 4). Goldstein also discloses a variable packet size (page

2, paragraph 21).

It would have been obvious to one of ordinary skill in the art, having the teachings of

Goldstein and Norman before him at the time the invention was made, to use the flash memory

resource management teachings of Goldstein in the memory system of Norman, in order to

provide memory management for electronic devices having limited and/or finite memory

resources (Goldstein, page 1, paragraph 7).

Alternatively, it would also have been obvious to one of ordinary skill in the art, having

the teachings of Goldstein and Norman before him at the time the invention was made, to use the

bit inversion teachings of the flash memory system of Normal in the digital camera system of

Goldstein, in order to reduce power consumption (col. 7, lines 1 – 4), reduce average time to

write (col. 7, 37 – 39), and to increase the average life time of the array's cells (col. 7, lines 39 –

40).

Response to Amendment

37.   Claim 13 has been amended to overcome rejections of claims 13 – 16 under 35

U.S.C. 101 and 35 U.S.C 112, second paragraph. This amendment seems to have overcome the

rejections. Accordingly, corresponding rejections are withdrawn.

Response to Arguments

38.   Applicant's arguments have been considered but are moot in view of the new ground(s)

of rejection.

Conclusion

40.   Any inquiry concerning this communication or earlier communications from the
examiner should be directed to Woo H. Choi whose telephone number is (571) 272-4179. The
examiner can normally be reached on M-F, 9:00-5:30.

        If attempts to reach the examiner by telephone are unsuccessful, the examiner's
supervisor, Matt Kim can be reached on (571) 272-4182. The fax phone number for the
organization where this application or proceeding is assigned is 703-872-9306.

        Information regarding the status of an application may be obtained from the Patent
Application Information Retrieval (PAIR) system. Status information for published applications
may be obtained from either Private PAIR or Public PAIR. Status information for unpublished
applications is available through Private PAIR only. For more information about the PAIR
system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR
system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Woo H. Choi
June 22, 2005